

DATA PROCESSING SYSTEM HAVING AN ADAPTIVE PRIORITY CONTROLLER

Abstract of the Disclosure

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The present invention relates generally to data processors and more specifically, to data processors having an adaptive priority controller. One embodiment relates to a method for prioritizing requests in a data processor (12) having a bus interface unit (32). The method includes receiving a first request from a first bus requesting resource (e.g. 30) and a second request from a second bus requesting resource (e.g. 28), and using a threshold corresponding to the first or second bus requesting resource to prioritize the first and second requests. The first and second bus requesting resources may be a push buffer (28) for a cache, a write buffer (30), or an instruction prefetch buffer (24).

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15 According to one embodiment, the bus interface unit (32) includes a priority controller (34) that receives the first and second requests, assigns the priority, and stores the threshold in a threshold register (66). The priority controller (34) may also include one or more threshold registers (66), subthreshold registers (68), and control registers (70).

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